Abstract— FPGA have always taken benefit of the most advanced technology nodes for offering better performance than CPU and better time-to-market than ASSP. However, with the slow-down of technologies and its exponentially increasing cost, FPGA race towards better integration is nowadays compromised. One alternative path to scaling is to go 3D. This promising solution can offer scaling at a lower cost while solving some FPGA issues such as yield or I/Os management. However, 3D solutions come with some drawbacks with heterogeneous performances of 3D/2D links and limited 3D interconnections. In this paper, we show some recent advances on the usage of 3D technologies for enhancing FPGA capacities.

Keywords— FPGA, 3D, TSV, monolithic integration

I. 3D TSV INTEGRATION

Application requirements have always been more and more aggressive for FPGAs. Advanced technologies classically helped FPGA gain better performance. Recent ITRS reports show that scaling is reaching its limits due to the difficulties and exponentially increasing cost of process in advanced nodes (eg. double patterning). A strong candidate to keep increasing the logic density is to explore the opportunities of 3D integration.

Parallel integration, with the use of Through-Silicon Vias (TSVs) makes possible to integrate separately fabricated dies vertically. With TSV integration, FPGAs can gain in terms of area and performance. In [3], different 3D switchbox topologies are surveyed for TSV-based FPGAs with several layers. Since more complex switchboxes are required, the improvement of delay is limited. Delay reduction of 10% is achievable for two-layer integration and 24% for five-layer. There are several works which focus on decreasing the number of TSVs in order to reduce area and delay [4]. EDP reduction up to 44% is achieved when four layers are integrated. Silicon interposers are proposed as a low cost solution node between 2D and 3D. FPGA vendor Xilinx has released an FPGA fabricated on interposer [5] with reduced TSV aspect ratio of 10 in order to increase yield.

In all this literature, 3D-TSV integration has demonstrated limited impact on FPGA and the only current application is on yield improvement. One reason is probably the interconnection-dominated nature of FPGA which implies a need of 3D interconnection that TSV integration cannot offer right now. As a result, other 3D solutions must be investigated. In this paper, we discuss two innovative 3D solutions and their potential impact on FPGA: monolithic integration (3DMI) and vertical NW-FET.

II. 3DMI INTEGRATION

Recent ITRS roadmap [1] shows that TSV alignment performance will be limited in between ~ 0.5 - 1µm (Table I). Due to the restriction in the alignment, the pitch between two TSVs cannot be smaller than ~ 4 - 8µm. In addition, the depth of TSV (~ 20 - 50 µm) implies performance impact when signals crossing TSV are on the chip critical paths. Consequently, the number of TSVs between two layers can only support coarse grain partitioning. On the other hand, in 3D Monolithic Integration (3DMI), transistor layers are fabricated one after another on the same die (Figure 1). It results in an improved alignment performance of ~10nm [2]. Moreover, the distance between the top and bottom layers can be reduced down to 23nm [2], decreasing the delay while passing through the 3D via.

TABLE I. 3DMI VS TSV VERTICAL CONNECTION COMPARISON

<table>
<thead>
<tr>
<th></th>
<th>Alignment (µm)</th>
<th>Diameter (µm)</th>
<th>Pitch (µm)</th>
<th>Minimum Depth(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV</td>
<td>0.5 – 1</td>
<td>2 - 4</td>
<td>4 - 8</td>
<td>20 – 50</td>
</tr>
<tr>
<td>3DMI</td>
<td>0.01</td>
<td>0.035</td>
<td>0.08</td>
<td>0.05</td>
</tr>
</tbody>
</table>

3DMI vs. TSV gain

|                  | 50x – 100x    | 57x – 114x    | 50x – 100x    | 400x – 1000x     |

Fig. 1. Cross-sectional view of multi-tier 3D monolithic integration.

Recently, a number of works focused on monolithically integrated FPGAs. In [6], authors show improvements depending on several different stacking scenarios of logic and memory layers. Up to 42% delay and power reductions can be achieved with 69% smaller area when three layers are considered with down-scaled memory cell. In [7], a switchbox with memory and logic separation is presented with 20% smaller area and 22% reduced delay. In [8], a 3D FPGA with logic-on-memory approach is presented with 47% reduced EDP in a 55% smaller area.
III. 3D NW-FET

Five-year old works have demonstrated the possibility to grow single crystalline silicon nanowires on a metallic line [9]. This work represents a great opportunity to build FET devices in the interconnect levels (Figure 2). Using chemical vapor deposition nanowire growth, in-situ doping and low temperature conformal depositions, it is possible to integrate these nanowires into vertical transistors [10,11] connecting metallic lines.

In FPGAs, more than 50% of the resources are used for routing, leading in a large overhead in terms on area. Using the proposed 3-D technology, all routing switches, associated buffers and memories can be implemented in the routing layers. An evaluation of the potential gains using MCNC benchmarks and the VPR tool flow has been performed in [12]. An area saving of about 46.2% thanks to the decrease of the area allocated to routing is observed. Finally, the benchmarks show a delay reduction ranging from 37% to 48%, with 42% on average.

IV. CONCLUSION

3D TSV is neither the only 3D technology for FPGA implementation nor the most promising one. In this paper, we have shown two other promising 3D technologies for FPGA design, and their potential gains, opening the path to real 3D FPGA implementation.

REFERENCES